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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,168	12/22/2000	Ananda Sarangi	42390.P9470	2325

7590 11/17/2003

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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2185	10

DATE MAILED: 11/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/746,168	Applicant(s) SARANGI ET AL.	
	Examiner James K. Trujillo	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Declaration and Fee dated 2/26/01, Drawing 5/21/01, Petition 1.53 dated 5/29/01, Petition 1.182 dated12/17/01, CFR dated 8/22/02.

2. Claims 1-20 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "A processor comprising: front-end logic to receive a control signal; and configuration logic coupled to the front-end logic to inhibit booting up..." as per claim 11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 16 objected to because of the following informalities: As to claim 16, on line 5, "on" should be changed to one. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As to claim 1, claim 1 recites on line 10 "a proper fuse block voltage". It appears that this voltage can be interpreted as either a control signal having an appropriate voltage level or that the fuse block is supplied by a voltage that has a proper supply voltage level. For purposes of examination the latter will be interpreted be the limitation in claim 1.

8. As to claims 2-5, they are dependent upon claim 1 and are therefore also rejected.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-8, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, U.S. Patent 5,951,681 in view of Gunderson et al., U.S. Patent 6,433,405 and Keehn et al., U.S. Patent 5,630,090.

11. As to claim 1, Chang substantially taught in figures 1, 2, 5, 6 and 7, as per claim 1, a voltage regulator (voltage converters 13, 131) and clock generator (frequency generator 20) to send a processor voltage or a processor clock respectively.

Chang also taught in same figures a processor (CPU 10) coupled to the voltage regulator to receive the processor voltage and the clock generator to receive the processor clock, respectively.

Chang further taught a control signal coupled to the processor, the voltage regulator (signal from voltage controller to voltage converter) and a control signal coupled to the processor and the clock generator (frequency generator, the clock is controlled by a signal from the frequency controller) to prevent (preventing an incorrect setting of voltage and frequency from destroying the processor) the processor from receiving the processor voltage and the processor clock until a voltage configuration signal and frequency configuration signal to specify the processor voltage and the processor clock frequency (new user settings for CPU) [figures 1, 2 and 7, col. 5 lines 24-63].

Chang does not expressly disclose a single control signal. Chang also does not expressly disclose a fuse block programmed the voltage configuration and the frequency configuration to specify the processor voltage and clock frequency. Chang does not expressly disclose wherein the fuse block has a proper voltage.

As to the control lines, Chang uses two control signals instead of a single control signal, one for the clock and one for the voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang by integrating both control signals. An artisan would have made the modification to reduce the number of control lines thereby reducing space required for the invention.

As to the fuse block, in summary, Chang teaches, in col. 2, lines 1-43, using a storage device programmed with the voltage configuration (settings) and frequency configuration (settings) to specify the processor voltage and clock frequency.

Gunderson teaches, in col. 2, lines 13-29, using a fuse block as storage device to store specific configuration (operational) information for an integrated circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang by using the fuse block as taught by Gunderson to store the frequency and voltage configuration. An artisan would have been motivated because Gunderson teaches, at col. 3, lines 20-34, that his fuse block desirably increases the probability that the programming will be successful.

As to the fuse block having a proper voltage, Keehn teaches a system wherein the memory is determined to have a proper voltage (the memory becomes activated) and prevent the processor from accessing it (the memory becomes activated before the process accesses it) [col. 7 lines 12-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination of Chang and Gunderson by preventing the processor from accessing the fuse block containing configuration signal until the fuse block has a proper voltage because the fuse block is a type of memory as taught by Keehn. An artisan would have made the modification to ensure that correct data was supplied to the processor.

12. As to claim 2, Chang together with Gunderson and Keehn taught the system according to claim 1. In summary, as combined, once the fuse block has a proper voltage the processor would be allowed to receive voltage and clock signals. Chang together with Gunderson and Keehn do not expressly disclose wherein the voltage regulator is coupled ***to send the fuse block voltage to***

the processor and the control signal to the processor and the clock generator [emphasis added]. However, it is well known in the computer arts that the processor and memory, such as a fuse block, operate with the same logic voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang together with Gunderson and Keehn to have the voltage regulator send the fuse block voltage to the processor. An artisan would have made the modification because the voltage regulator supplies the voltage and the memory and processor operate with the same voltage thus reducing the number of power rails.

13. As to claim 3, Chang together with Gunderson and Keehn taught the system according to claim 1 as described above. Chang taught a second voltage regulator (voltage converter 132) [figures 6 and 7]. Chang together with Gunderson and Keehn do not expressly disclose wherein the second voltage regulator is coupled ***to send the fuse block voltage to the processor*** and the control signal to the processor and the clock generator [emphasis added]. However, it is well known in the computer arts that the processor and memory, such as a fuse block, operate with the same logic voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang together with Gunderson and Keehn to have the second voltage regulator send the fuse block voltage to the processor. An artisan would have made the modification because the voltage regulator supplies the voltage and the memory and processor operate with the same voltage thus reducing the number of power rails.

14. As to claim 4, Chang together with Gunderson and Keehn taught the system according to claim 1 as described above. Chang taught a second voltage regulator (voltage converter 132) [figures 6 and 7]. Chang together with Gunderson and Keehn do not expressly disclose wherein the ***second voltage regulator*** is coupled ***to send the fuse block voltage to the processor*** and the

first voltage regulator is coupled to ***sense the fuse block voltage and to send the control signal*** to the processor and the clock generator [emphasis added]. However, it is well known in the computer arts that the processor and memory, such as a fuse block, operate with the same logic voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang together with Gunderson and Keehn to have the second voltage regulator send the fuse block voltage to the processor and have the first voltage regulator sense the fuse block voltage and to send the control signal to the processor and clock generator. An artisan would have made the modification because the voltage regulator supplies the voltage and the memory and processor operate with the same voltage thus reducing the number of power rails.

15. As to claim 5, Chang together with Gunderson and Keehn taught the system according to claim 1 as described above. Neither Chang nor Gunderson taught the system further comprising a transistor coupled to invert the control signal and send the inverted control signal to the clock generator. Chang teaches sending the control signal to the frequency controller but does not invert the signal.

Official Notice is taken of signal inversion to accommodate a logic system with either positive or negative logic. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a transistor to invert the control signal to the clock generator because it is well known in the art that inverting the signal is not a significant change and are essentially equivalent.

16. As to claim 6, Chang taught, in figures 1, 2, 5-7, at col. 2, lines 31-59, col. 3, lines 35-38 and at col. 4 lines 47-48 a system comprising:

a. a processor coupled to a storage device with at least one configuration signal (voltage and frequency);

b. logic (controllers) coupled to the processor to read the configuration signal and in response to generate a value specified by the configuration signal (a particular voltage and frequency).

Chang does not expressly disclose a programmable fuse block programmed configuration signal. Chang teaches, in col. 2, lines 1-43, using a storage device programmed with the configuration signals (frequency and voltage settings). Chang also does not expressly disclose a control signal coupled to the processor and the logic to prevent the logic from reading the configuration until a predetermined event occurs.

Gunderson teaches, in col. 2, lines 13-29, using a fuse block as storage device to store specific configuration (operational) information for an integrated circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang by using the fuse block as taught by Gunderson to store the frequency and voltage configuration. An artisan would have been motivated because Gunderson teaches, at col. 3, lines 20-34, that his fuse block desirably increases the probability that the programming will be successful.

Keehn teaches a system having control signal coupled to the processor and the logic to prevent the logic from reading the configuration until a predetermined event occurs [col. 7 lines 12-15]. Specifically, the control signal of Keehn is a signal determining that the memory becomes activated. Until the memory is activated the system prevents the processor from accessing it.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination of Chang and Gunderson by preventing the processor from accessing the fuse block containing configuration signal until the fuse block has a proper voltage because the fuse block is a type of memory as taught by Keehn. An artisan would have made the modification to because waiting until the proper voltage for the memory would ensure that correct data was supplied to the processor from the memory.

17. As to claims 7 and 8, Chang together with Gunderson and Keehn taught the system according to claim 6 described above. Chang further taught wherein the configuration signals specify a voltage and a frequency for the logic to generate.

18. As to claim 9, Chang together with Gunderson and Keehn taught the system according to claim 6 described above. Chang taught wherein the predetermined event is when the configuration signal is valid and stable [col. 3, lines 35-38 and at col. 4 lines 47-48]. The fuse block must be valid and stable before any information is read they are read. Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang by ensuring that the fuse block was valid and stable before data is read from it. An artisan would have made the modification because if the fuse block were not stable corrupted data would be read from the fuse block, which is highly undesirable.

19. As to claim 10, Chang together with Gunderson and Keehn taught the system according to claim 6 described above. Chang taught wherein the predetermined event is when the configuration signal is valid and stable [col. 3, lines 35-38 and at col. 4 lines 47-48]. The signals must be valid before they are read. Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang by ensuring that the configuration

data was valid and stable before data is read from it. An artisan would have made the modification because if the configuration data were not stable corrupted configuration data would be read, which is highly undesirable.

20. As to claim 14-20, Chang together with Gunderson and Keehn taught the claimed system therefore together they also taught the claimed instructions in a machine-readable medium to operate the system.

21. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, U.S. Patent 5,951,681.

22. As to claim 11-13, Chang taught a system comprising:

a. front-end logic (detection unit) to receive a control signal (the state) [col. 5 lines 53-63]; and

b. configuration signal logic (to determine if the state data should be abandoned) coupled to the front-end logic to inhibit booting up (stop the boot while the user sets the new state data) of the processor in response to the front-end logic receiving the control signal.

Specifically, Chang taught front-end logic that receives a control signal. The control signal is passed to configuration logic, which then inhibits booting if the voltage and frequency is not compatible with processor that has just been inserted. During the boot inhibit, a user is allowed to enter new settings [col. 5 lines 53-63].

Chang does not expressly disclose wherein all the front-end logic and configuration signal logic is on a processor. Chang taught where logic units are separate devices and not on a

processor. It is well known in the electrical and computer arts to integrate devices. Integrating devices increases reliability and lowers costs. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Chang by integrating all of the logic onto the processor to desirably improve reliability and lower costs.

23. As to claim 12, Chang as modified taught the processor according to claim 11 described above. Chang further taught wherein the configuration signal logic is to inhibit booting up of the processor for a period of time. Specifically, Chang taught that during the boot incorrect setting are prevented (stopping the boot) from destroying the CPU and the user is allowed to change the settings.

24. As to claim 13, Chang as modified taught the processor according to claim 11 as described above. Chang further taught wherein the configuration signal logic is coupled to the front-end logic to inhibit booting up of the processor for a period of time after the configuration signal logic has power. Specifically, in Chang the configuration logic must be powered for a period of time before it inhibits the booting because it must first determine if the voltage and frequency are appropriate.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

> U.S. Pat. No. 5,862,351 to He. This patent teaches a system that allows different operational parameter to be used for different processors with the same motherboard.

U.S. Pat. No. 6,567,868 to Tran et al. This patent teaches a system that automatically sets CPU speed.

Japan Pat. No. JP407200526 A to Sugihara. This patent teaches changing the access frequency of a CPU.

Aggarwal, G.; Thaper, N.; Aggarwal, K.; Balakrishnan, M.; Kumar, S.; "A novel reconfigurable co-processor architecture", VLSI Design, 1997. Proceedings., Tenth International Conference on, 4-7 Jan. 1997. This paper teaches reconfiguring a co-processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
November 6, 2003

THOMAS LEE
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